AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph under the Specification heading "ABSTRACT" with the following amended paragraph:

~~The present invention describes an~~ An integrated image detecting apparatus with low noise is provided. [[,]] ~~which~~ The apparatus transforms optical current ~~to~~ into voltage and ~~comprises~~ includes an optical detecting element, an ~~integrated~~ integrator circuit, a correlated double sampling circuit, and an output circuit. The ~~present invention is a~~ apparatus adopts CMOS process and is designed for different CMOS image application systems. [[,]] ~~which~~ The apparatus keeps the advantages of low power consumption and ~~better~~ superior integration ability and is able to eliminate the shifts [[.]] ~~Shifts~~ of circuit characteristics caused by process variation ~~are furthermore eliminated~~.

Please replace paragraph [0002] with the following amended paragraph:

[0002] The present invention is an integrated image detecting apparatus, and especially relates to ~~the one~~ an integrated image detecting apparatus with low noise that transforms ~~transforming~~ optical current ~~to~~ into voltage [[.]] ~~The~~ and is capable of improving the

problem of ~~deficient~~ poor sensitivity and high random noise ~~occurred~~ which occurs with the high-speed operation of CMOS image chips.

Please replace paragraph [0003] with the following amended paragraph:

[0003] The present invention provides an integrated image detecting apparatus with low noise, which transforms optical current ~~to~~ into voltage and comprises an optical detecting element, an ~~integrated~~ integrator circuit, a correlated double sampling circuit, and an output circuit. The ~~integrated~~ integrator circuit and the correlated double sampling circuit will filter noise of signals output from the optical detecting element, then the A/N ratio will be improved substantially.

Please replace paragraph [0013] with the following amended paragraph:

[0013] Reference is made to Fig. 2, which shows a first embodiment of the present invention and comprises an optical detecting element 200, an ~~integrated~~ integrator circuit 210, a correlated double sampling circuit 230 and an output circuit 250. The optical

detecting element 200 is operated to detect an optical variation and converts the ~~photos~~ photons into charge, and can be realized implemented by a photodiode and the ~~integrated~~ integrator circuit 210 further comprises an operational amplifier 211, a reference voltage, an electric charge storing device, a CMOS switch 215, and an inverter 217 of CMOS. Where the reference voltage source one 219 is also included that control by external voltage source or a bias provided by certain circuit inside, and the electric charge storing device can be implemented as a capacitor 213. After the optical detecting element 200 transforms the received optical signals into current signals and inputs the current signals to the amplifier 211, which can be a single stage amplifier instead that consists of NMOS or PMOS transistors. The capacitor 213 is set across a negative input terminal and an output terminal of the amplifier 211. The CMOS switch 215 and the inverter 217 of the CMOS can be NMOS or PMOS transistors instead, and the CMOS switch 215 [[.]] is connected in parallel with the inverter 217 and across between the negative input terminal and the output terminal of the amplifier 211. A switch signal 218 is used to control the CMOS switch 215.

Please replace paragraph [0014] with the following amended paragraph:

[0014] Connecting a capacitor 231 and a single-stage buffer 233 to the output terminal of the ~~integrated~~ integrator circuit 210 makes up the correlated double sampling circuit 230. Thus, the ~~integrated~~ integrator circuit 210 is operated to convert charge produced by the optical detecting element 200 into an electronic signal that is in a different type voltage, which comprises a reset voltage operated while the switch ~~turning~~ turns on inside the ~~integrated~~ integrator circuit 210 and a bright voltage operated while switch ~~turning~~ turns off inside the ~~integrated~~ integrator circuit 210. The switch includes ~~a~~ an NMOS transistor turned on at high voltage and turned off at low voltage or a PMOS transistor turned on at low voltage and turned off at high voltage or a CMOS transistor turned on and turned off at both said high-low voltage. The single-stage buffer 233 is an output-stage buffer for the correlated double sampling circuit 230, which comprised an ac couple device, a CMOS switch, and a unit gain operational amplifier, and connects to read the electronic signal from the output of the ~~integrated~~ integrator circuit 210 for canceling variation of the optical detecting element 200 and of the ~~integrated~~ integrator circuit 210. ACMOS switch 235 and an inverter 237 are connected between the capacitor 231 and the single-stage buffer 233; a switch signal 238 controls a reference voltage source two 239 and it connects to the right of capacitor 231 which is ~~providing~~ provides the reference

voltage for the capacitor 231. The ac couple device mentioned above can be implemented as a capacitor, and the unit gain operational amplifier can be a single stage amplifier instead that be substituted for a plurality of NMOS or PMOS transistors.